Features...

- ■ Industry's first programmable logic device (PLD) incorporating System-on-a-Programmable-Chip™ integration
  - – MultiCore™ architecture integrating look-up table (LUT) logic, product-term logic, and embedded memory
  - – Embedded system block (ESB) implementation of product-term logic used for combinatorial-intensive functions
  - – LUT logic used for register-intensive functions
  - – ESB used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
- ■ High density
  - – 100,000 to 1 million typical gates (see Table 1)
  - – Up to 42,240 logic elements (LEs)
  - – Up to 540,672 RAM bits that can be used without reducing available logic
  - – Up to 4,224 product-term-based macrocells

Table 1. APEX 20K Device Features   *Notes (1), (2)*

Feature	EP20K100E EP20K100	EP20K160E	EP20K200E EP20K200	EP20K300E	EP20K400E EP20K400	EP20K600E	EP20K1000E
Maximum system gates	263,000	404,000	526,000	728,000	1,052,000	1,537,000	2,670,000
Typical gates	106,000	163,000	211,000	293,000	423,000	618,000	1,073,000
LEs	4,160	6,400	8,320	11,520	16,640	24,320	42,240
ESBs	26	40	52	72	104	152	264
Maximum RAM bits	53,248	81,920	106,496	147,456	212,992	311,296	540,672
Maximum macrocells	416	640	832	1,152	1,664	2,432	4,224
Maximum user I/O pins	252	320	382	420	502	620	780

Notes:

(1)   The embedded IEEE Std. 1149.1 JTAG boundary-scan circuitry contributes up to 52,130 additional gates.

(2)   This information is preliminary.

...and More Features

- Designed for low-power operation
  – 1.8-V and 2.5-V supply voltage (see Table 2)
  – MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, and 3.3-V devices (see Table 2)
  – ESB offering programmable power-saving mode
- Flexible clock management circuitry with phase-locked loop (PLL)
  – Built-in low-skew clock tree
  – Up to eight global clock signals
  – ClockLock™ feature reducing clock delay and skew
  – ClockBoost™ feature providing clock multiplication
  – ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  – Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  – Bidirectional I/O performance (t_{CO} + t_{SU}) up to 243 MHz
  – Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  – MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, and 3.3-V devices (see Table 2)
  – Programmable clamp to V_{CCIO}
  – Individual tri-state output enable control for each pin
  – Programmable output slew-rate control to reduce switching noise
  – Support for advanced I/O standards, including low-voltage differential signaling (LVDS), stub-series terminated logic (SSTL-3), and Gunning transceiver logic (GTL+)
  – Supports hot-socketing operation
  – Pull-up on I/O pins before and during configuration

Table 2. APEX 20K Supply Voltages

Feature	EP20K100 EP20K200 EP20K400	EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V	1.8 V, 2.5 V, 3.3 V

■ Advanced interconnect structure
  – Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  – Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  – Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  – Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect

■ Advanced packaging options
  – Available in a variety of packages with 144 to 984 pins (see Tables 3 through 6)
  – FineLine BGA™ packages maximize board space efficiency
  – SameFrame™ pin migration providing migration capability across device densities and package sizes

■ Advanced software support
  – Software design support and automatic place-and-route provided by the Altera® Quartus™ development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  – Altera MegaCore™ functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  – NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  – Quartus SignalTap™ embedded logic analyzer simplifying in-system design evaluation by giving access to internal nodes during device operation

Table 3. APEX 20K QFP, BGA & PGA Package Options & I/O Count   Notes (1), (2), (3)

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA	984-Pin PGA
EP20K100	101	159	189	252			
EP20K100E	92	149	181	✓			
EP20K160E	84	141	173	✓			
EP20K200		144	174	✓			
EP20K200E		134	166	✓	✓		
EP20K300E		118	150		✓		
EP20K400					502	502	
EP20K400E		100	132		✓		
EP20K600E					✓		
EP20K1000E							✓

Table 4. APEX 20K FineLine BGA Package & Footprint Migration Path   *Notes (1), (2), (3)*

Device	196-Pin	324-Pin	400-Pin	484-Pin	672-Pin	784-Pin
EP20K100	✓	✓	✓ (4)	✓ (4)	✓ (4)	✓ (4)
EP20K100E	✓	✓	✓ (4)	✓ (4)	✓ (4)	✓ (4)
EP20K160E			✓	✓ (4)	✓ (4)	✓ (4)
EP20K200				✓	✓ (4)	✓ (4)
EP20K200E				✓	✓	✓ (4)
EP20K300E					✓	✓ (4)
EP20K400					✓	✓ (4)
EP20K400E					✓	✓ (4)
EP20K600E					✓	✓
EP20K1000E						✓

Notes to tables:
(1) Consult Altera for up-to-date information on package availability and exact pin counts.
(2) I/O counts include dedicated input and clock pins.
(3) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
(4) All FineLine BGA packages, except the 196-pin package, are footprint-compatible via the SameFrame feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 65 for more information.

Table 5. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	936	1,197	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	35 × 35	45 × 45	62.5 × 62.5

Table 6. APEX 20K FineLine BGA Package Sizes

Feature	196-Pin	324-Pin	400-Pin	484-Pin	672-Pin	784-Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	225	361	441	529	729	841
Length × Width (mm × mm)	15 × 15	19 × 19	21 × 21	23 × 23	27 × 27	29 × 29

General Description

APEX 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions makes the APEX 20K architecture uniquely suited for System-on-a-Programmable-Chip design. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to one million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EPF20K1000E is an APEX 20KE device). Table 7 summarizes the features included in APEX 20K and APEX 20KE devices.

Table 7. Comparison of APEX 20K & APEX 20KE Features

Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
Hot-socketing support	Full support	Full support
SignalTap logic analysis	Full support	Full support
64-Bit 66-MHz PCI	Full compliance	Full compliance
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block
ClockLock support	Clock delay reduction 2× and 4× clock multiplication	Clock delay reduction $m/(n \times k)$ clock multiplication Drive ClockLock output off-chip External clock feedback LVDS support
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V I/O 3.3-V PCI LVCMOS LVTTL	1.8-V I/O 2.5-V I/O 3.3-V PCI 3.3-V AGP CTT GTL+ HSTL Class I, II, and III LVCMOS LVDS (in EP20K300E and larger devices) LVTTL SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the in-system programmability (ISP)-capable EPC2 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

☞   Contact Altera for information on future configuration devices.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by Altera's Quartus development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus software from within third-party design tools. Further, the Quartus software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus development system, includes DesignWare functions optimized for the APEX 20K architecture.

Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and first-in-first-out (FIFO) functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram
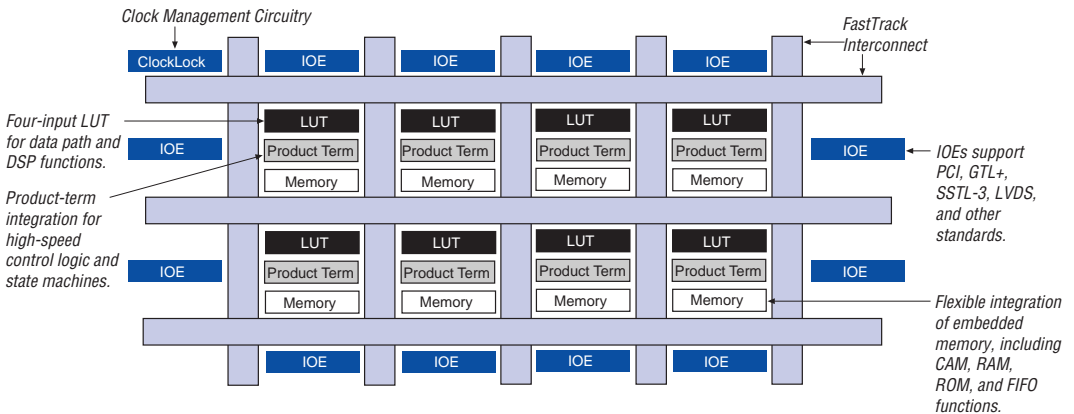
APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out.

APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins. APEX 20K devices also include ClockLock and ClockBoost clock management circuitry.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. Signals are routed between MegaLAB structures and to I/O pins via the FastTrack Interconnect. In addition, edge LABs can drive I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure
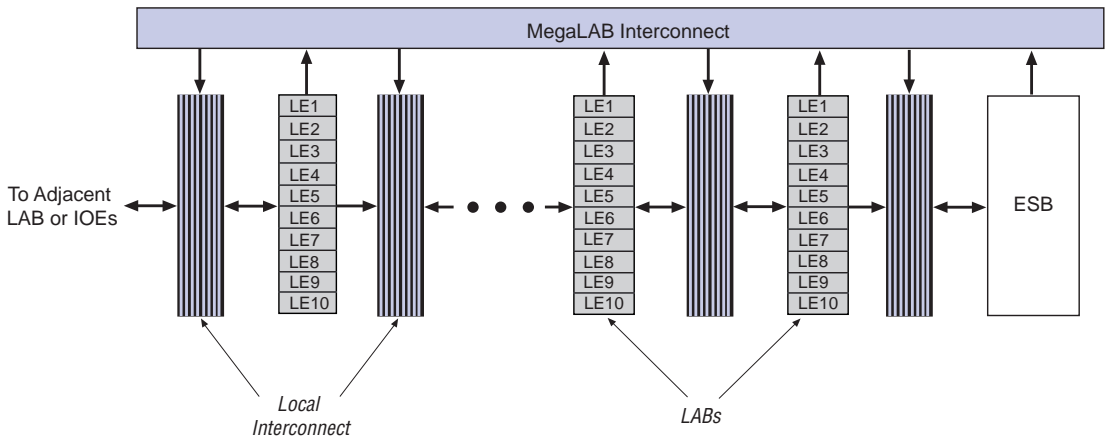
Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure
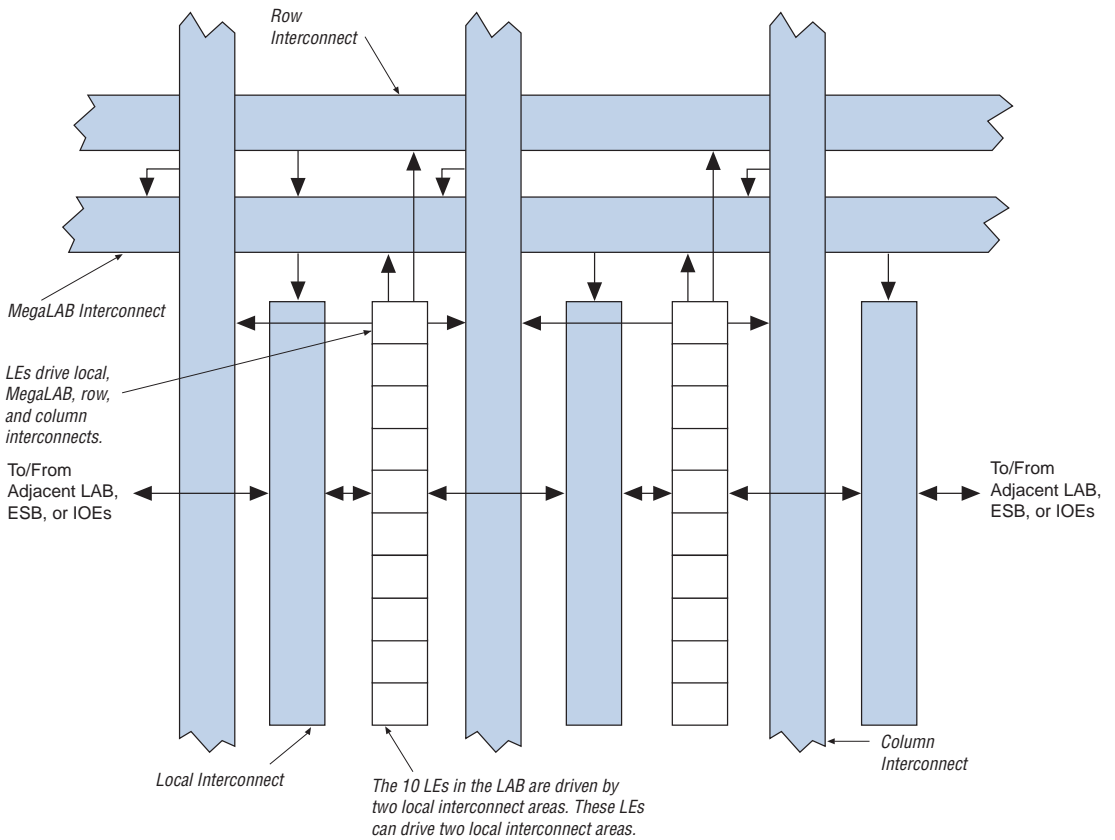
Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in an LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

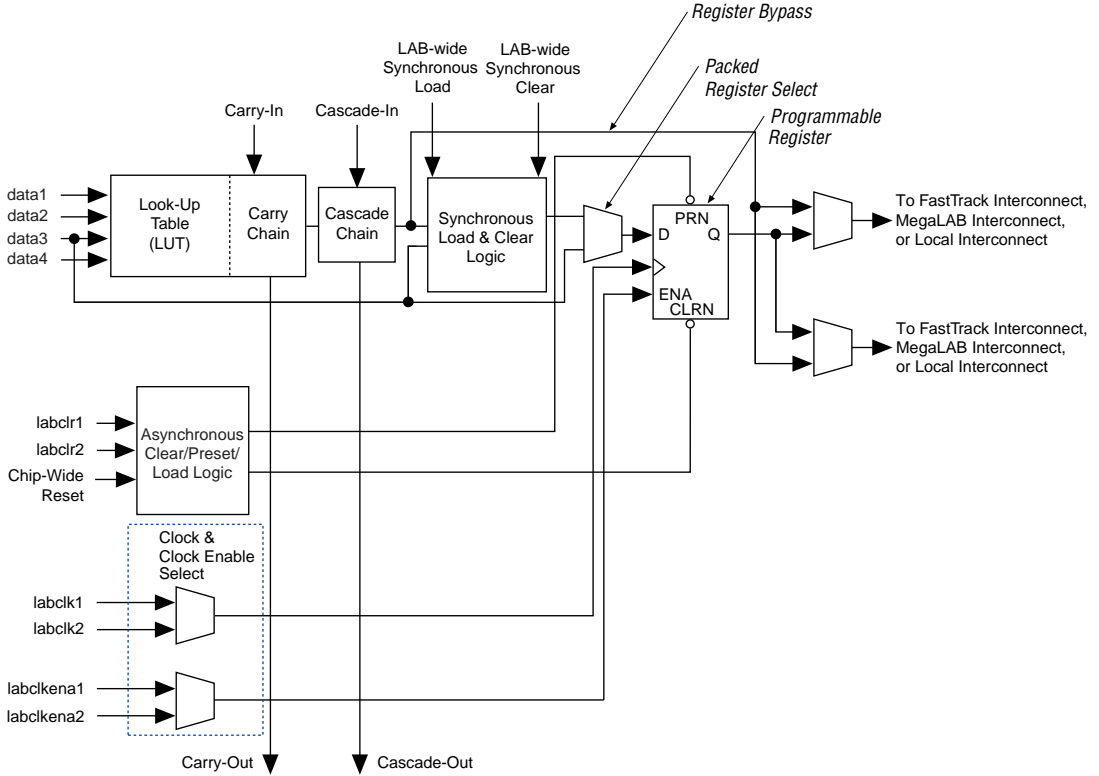*Figure 4. LAB Control Signal Generation*
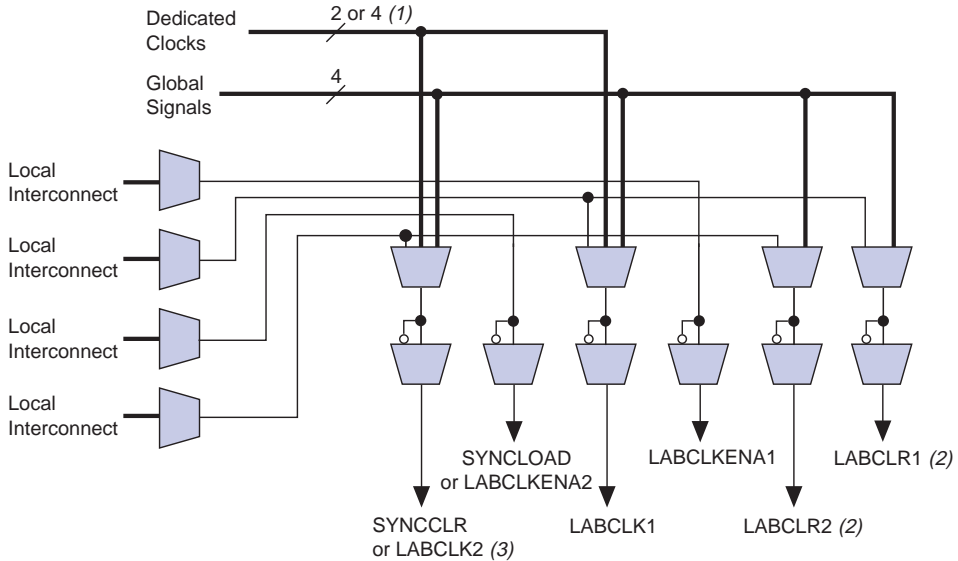
Notes:
(1)   APEX 20KE devices have four dedicated clocks.
(2)   The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
(3)   The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The logic element (LE), the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element

Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

The LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

*Figure 6. APEX 20K Carry Chain*
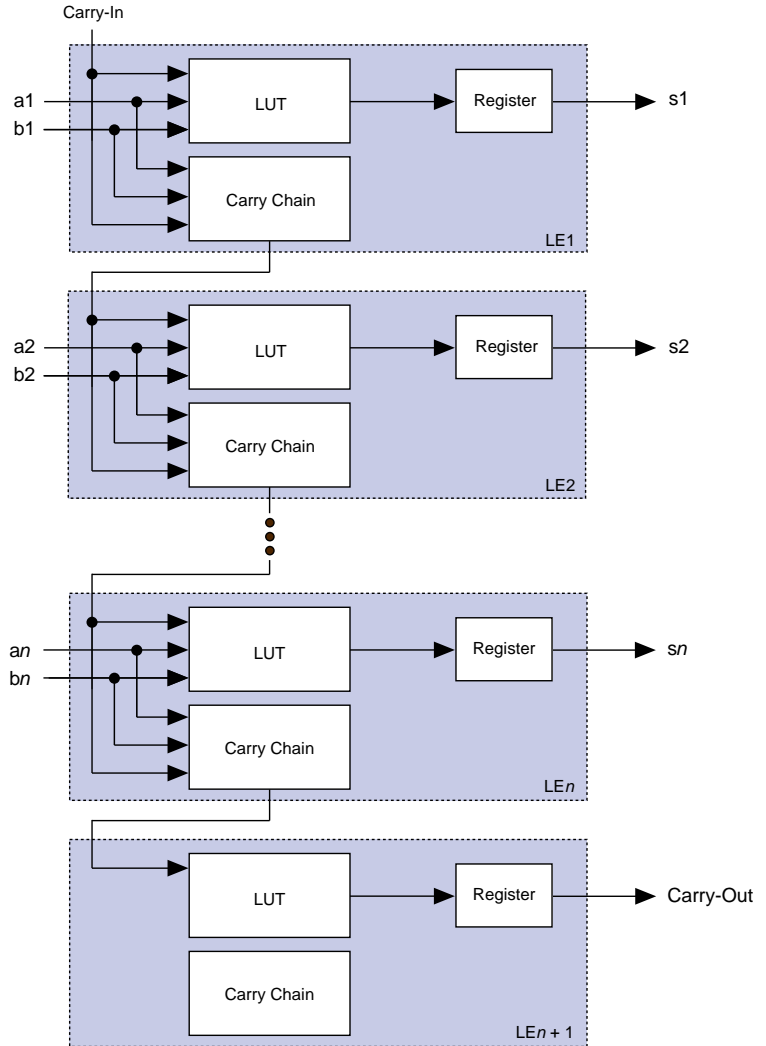
Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain
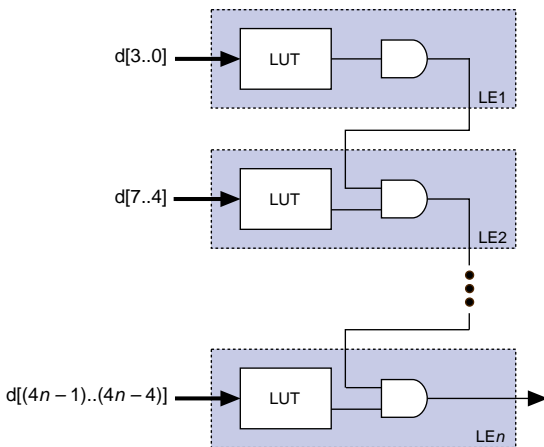
AND Cascade Chain   **OR Cascade Chain**
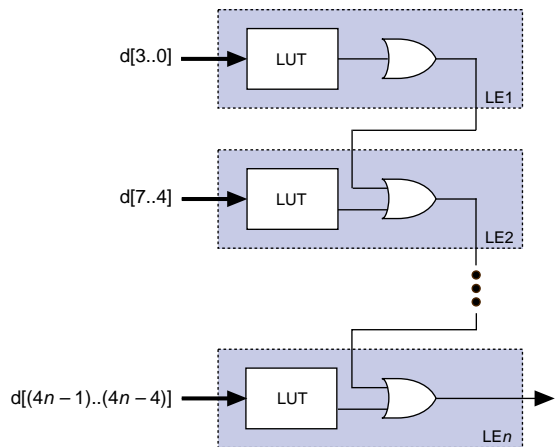
LE Operating Modes

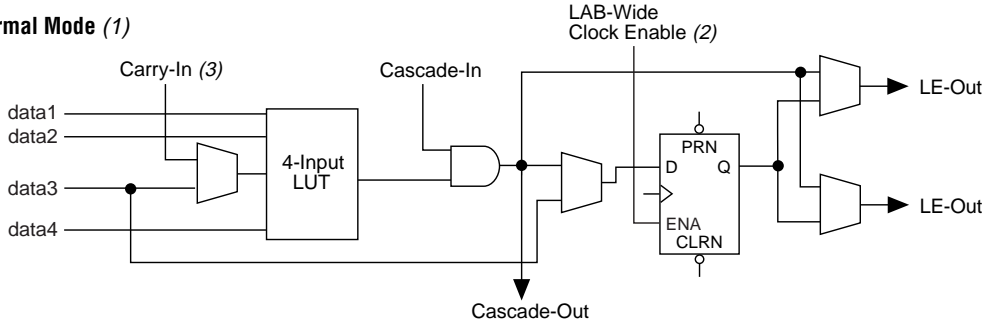The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.
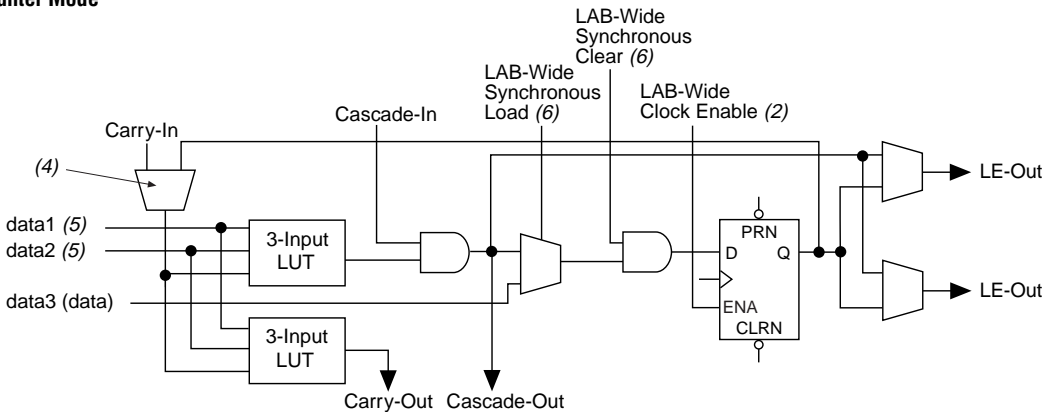
Figure 8. APEX 20K LE Operating Modes
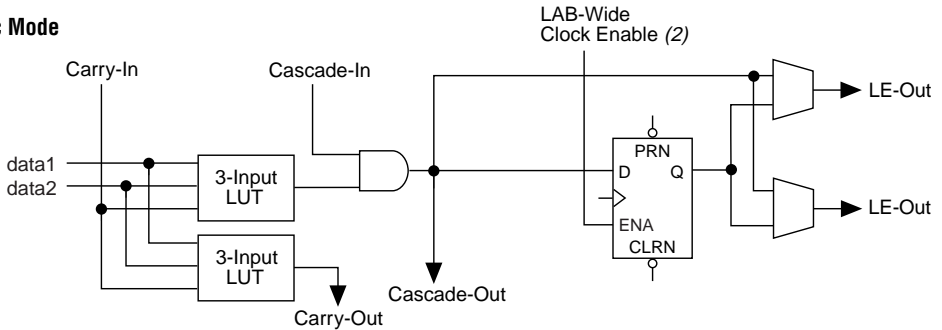
Notes:
(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a 4-input LUT. The Quartus Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a 3-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two 3-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (CHIP_RSTn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX 20K Interconnect Structure
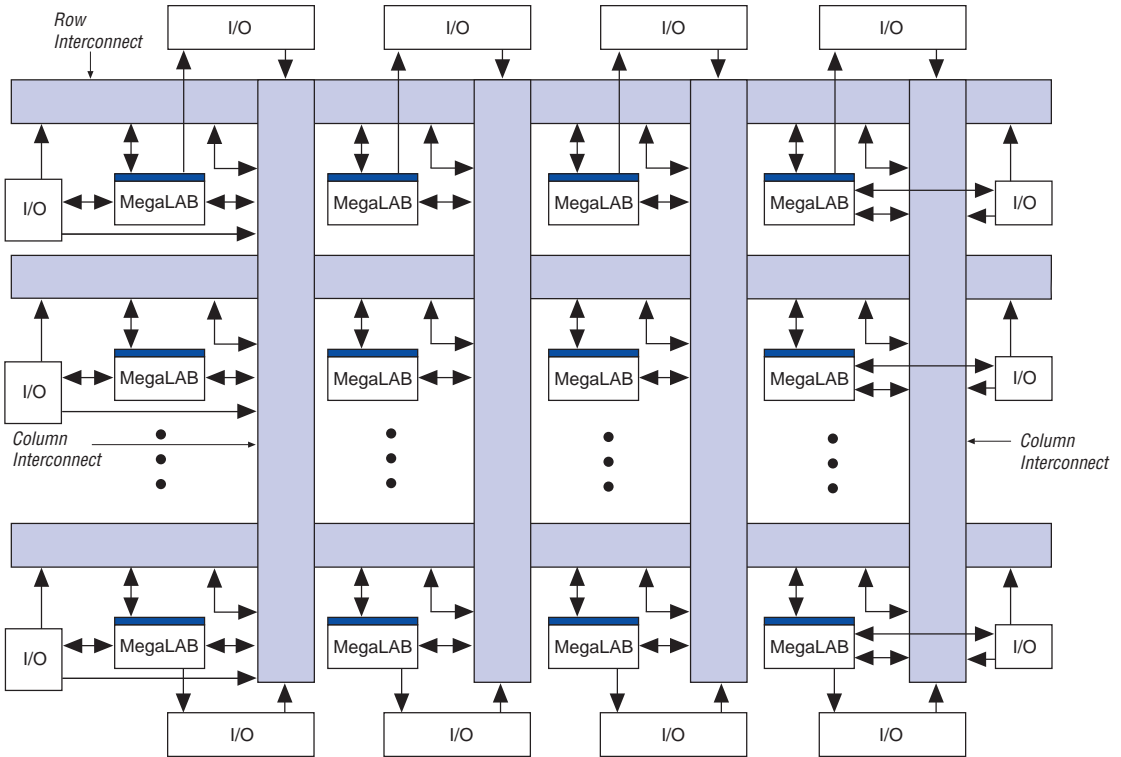
A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect
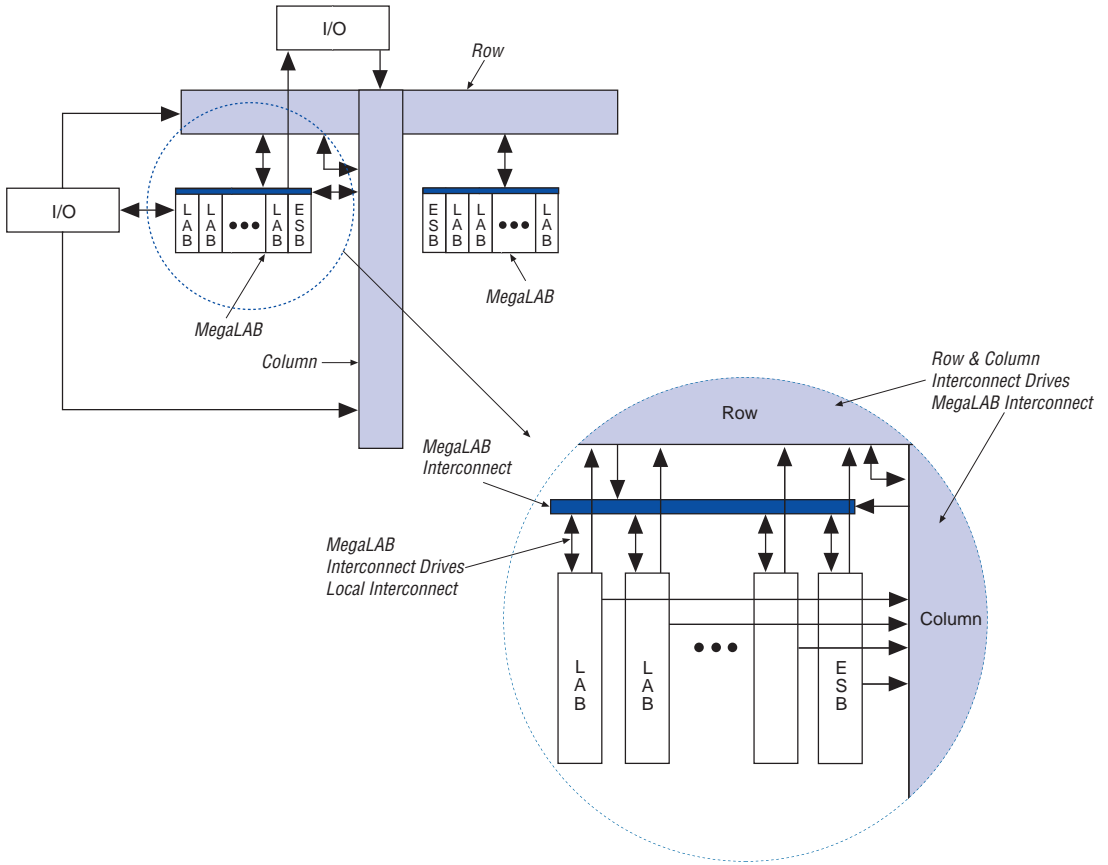

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect
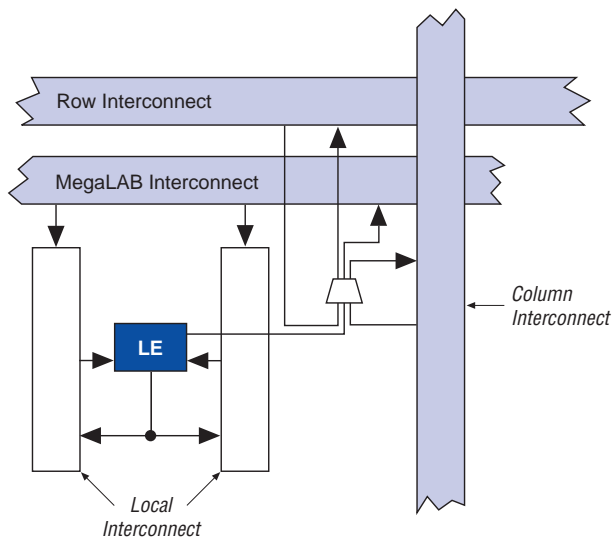
APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. Figure 12 shows the FastRow interconnect.

Figure 12. APEX 20KE FastRow Interconnect

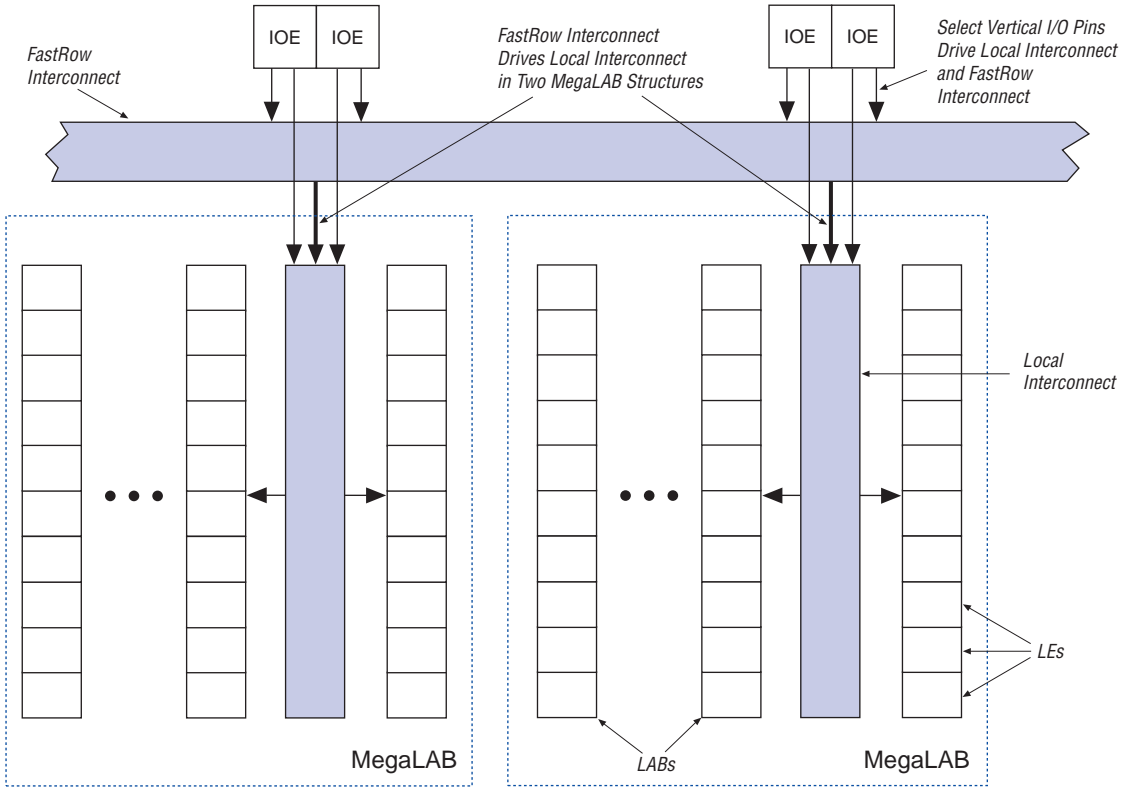Table 8 summarizes how various elements of the APEX 20K architecture drive each other.

Table 8. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin					✓ (1)			✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ (1)				

Note:
(1)   This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, 9 ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

Figure 13. Product-Term Logic in ESB
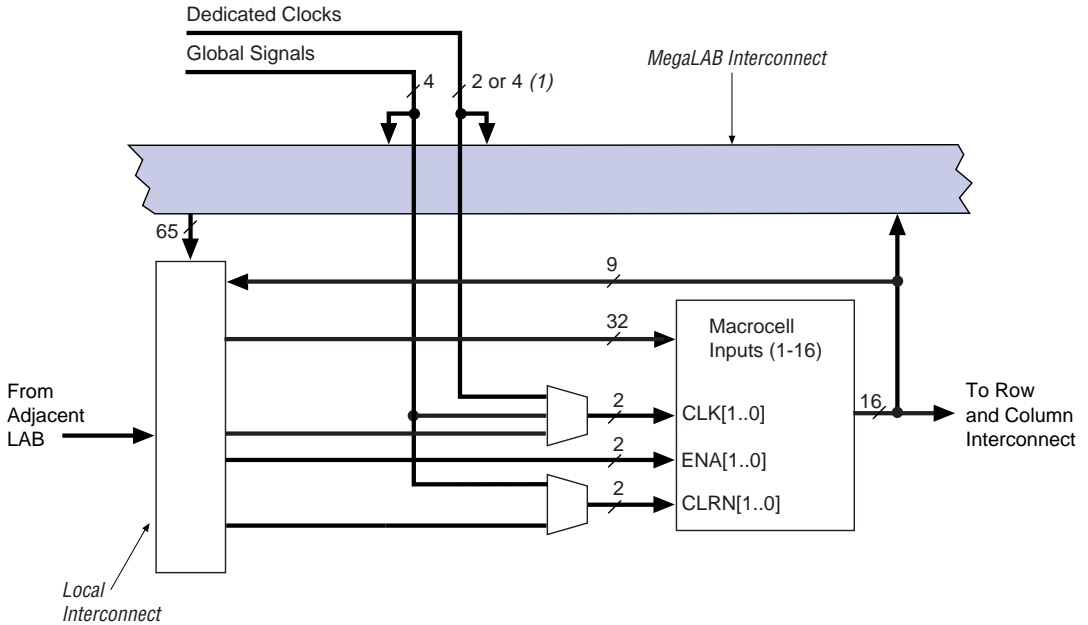
Note:
(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted: the Quartus software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

Figure 14. APEX 20K Macrocell
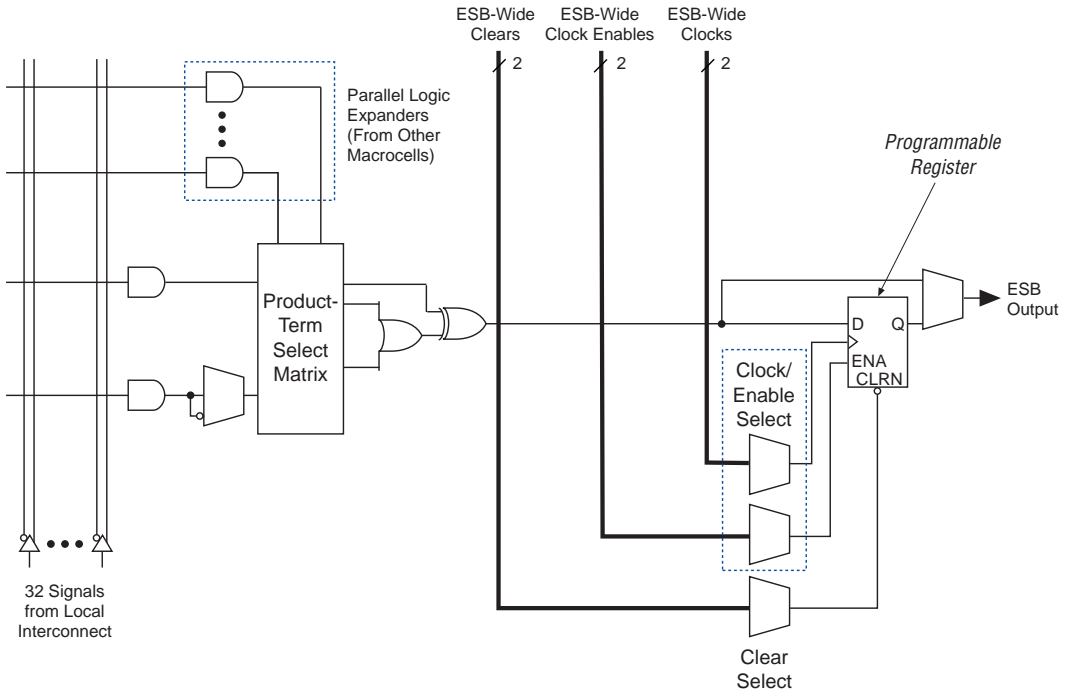
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic
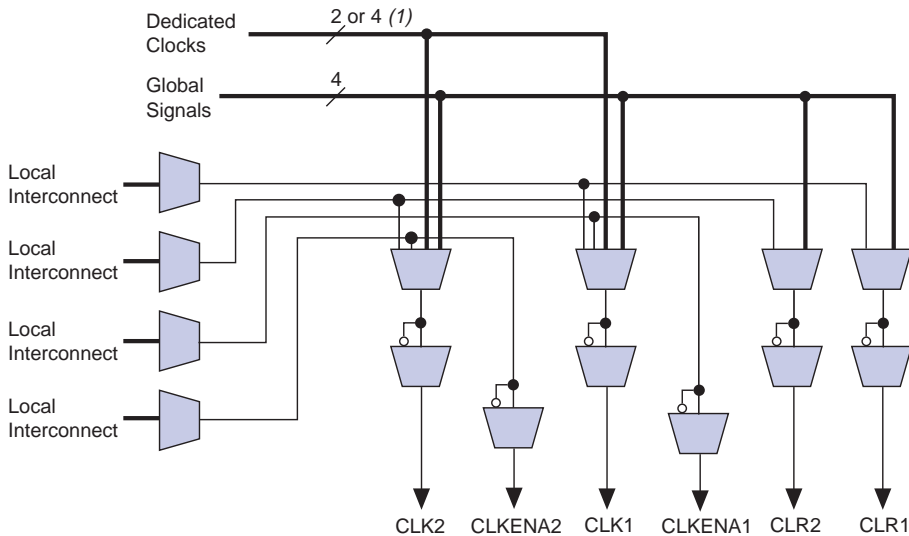
Note:
(1)   APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with 2 product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Figure 16. APEX 20K Parallel Expanders
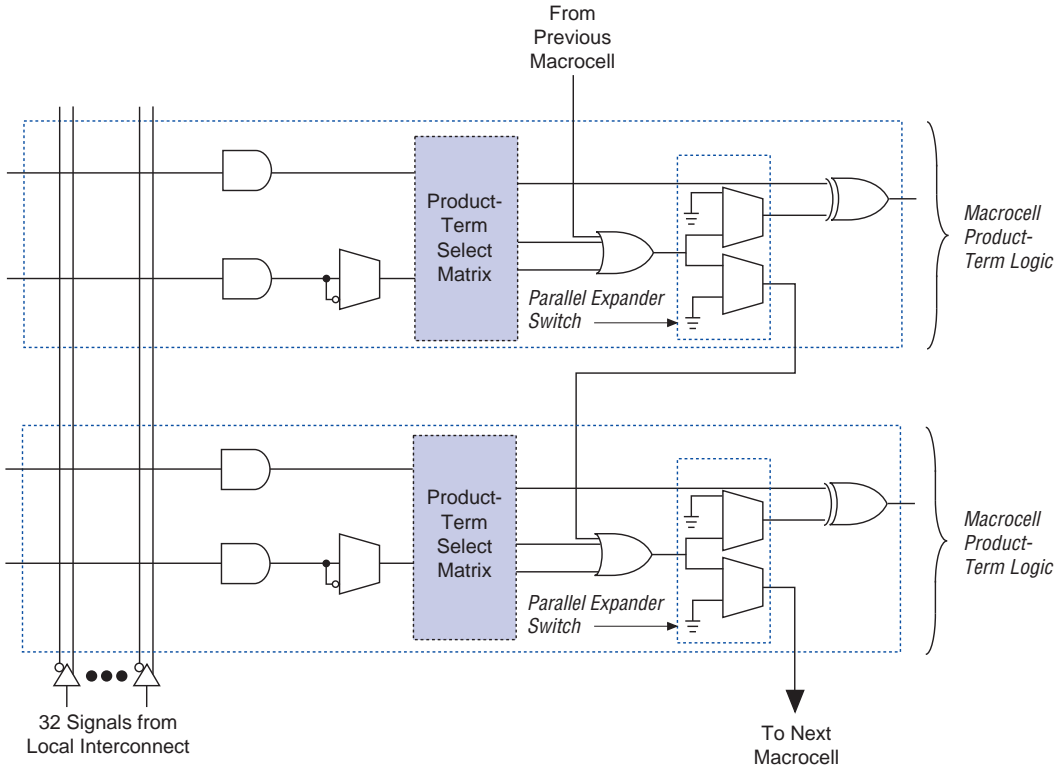
Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

Figure 17. ESB Block Diagram

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, 10 ESB outputs drive the local interconnect for fast connection to adjacent LEs or for fast feedback in product-term mode.

When used as memory, each ESB can be configured in any of the following sizes: 128×16, 256×8, 512×4, $1,024 \times 2$, or $2,048 \times 1$. By combining multiple ESBs, the Quartus software implements larger memory blocks automatically. For example, two 128×16 RAM blocks can be combined to form a 128×32 RAM block, and two 512×4 RAM blocks can be combined to form a 512×8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

Figure 18. Deep Memory Block Implemented with Multiple ESBs
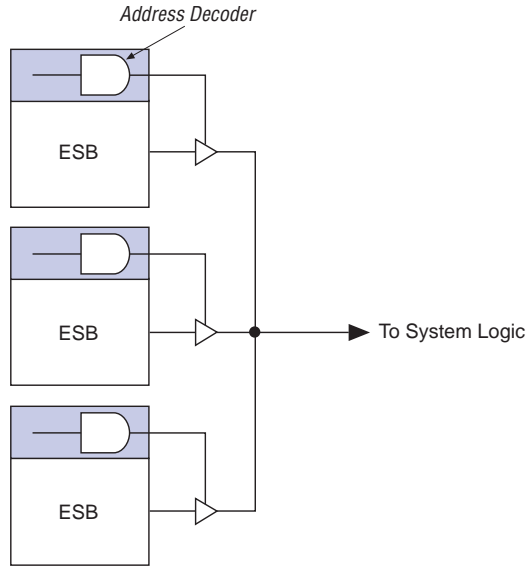
The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 19.

Figure 19. APEX 20K ESB Implementing Dual-Port RAM
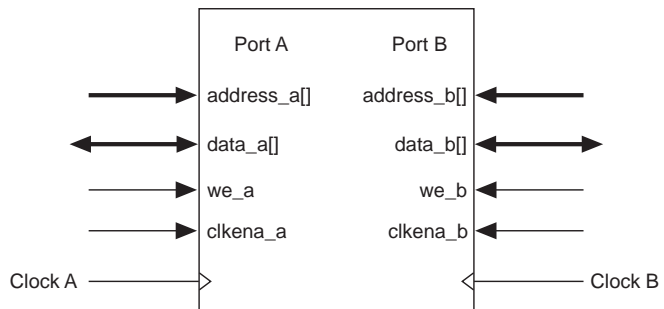
Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode   *Note (1)*
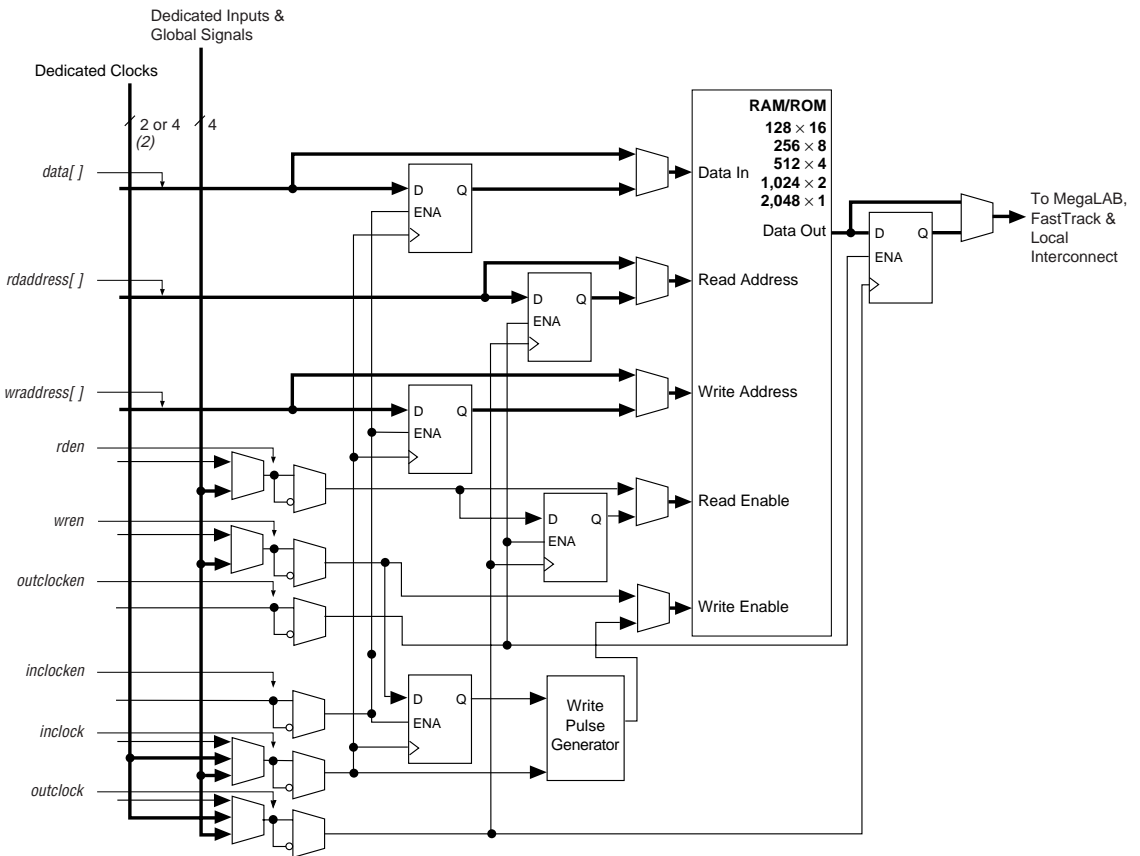
Notes:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode   *Note (1)*
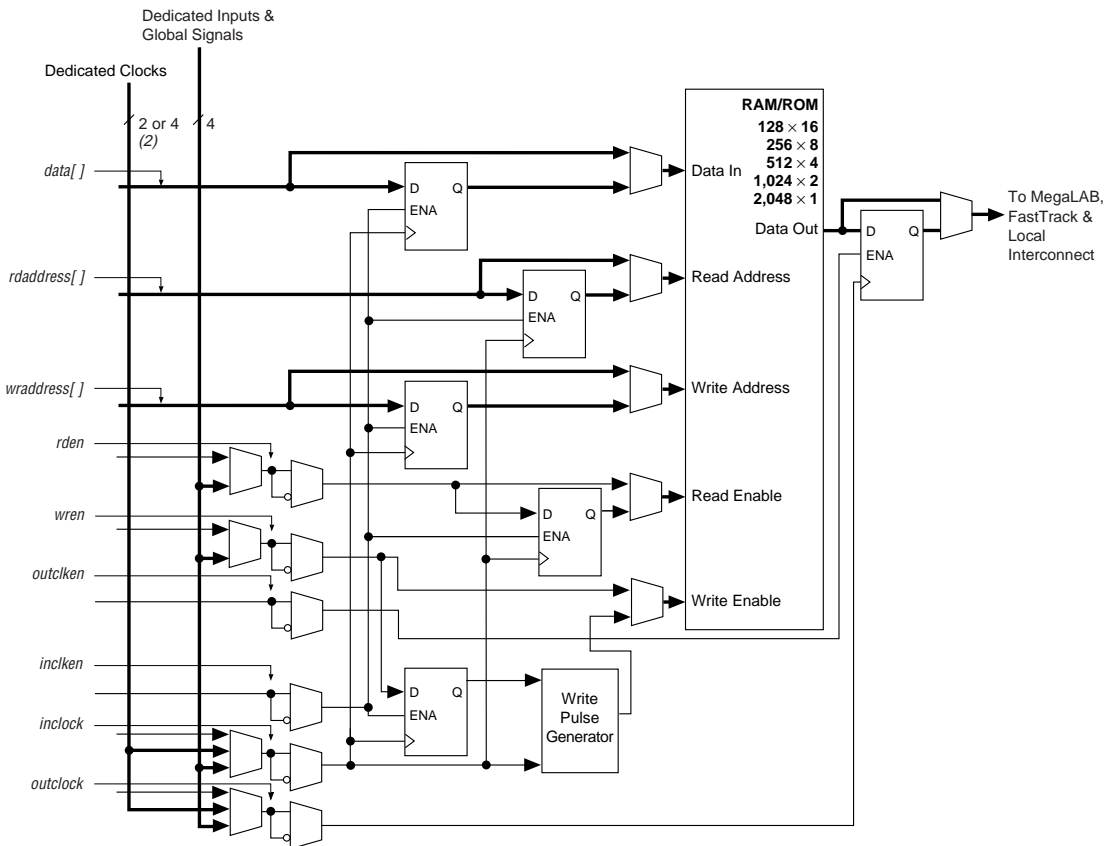
Notes:
(1)   All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2)   APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode   *Note (1)*
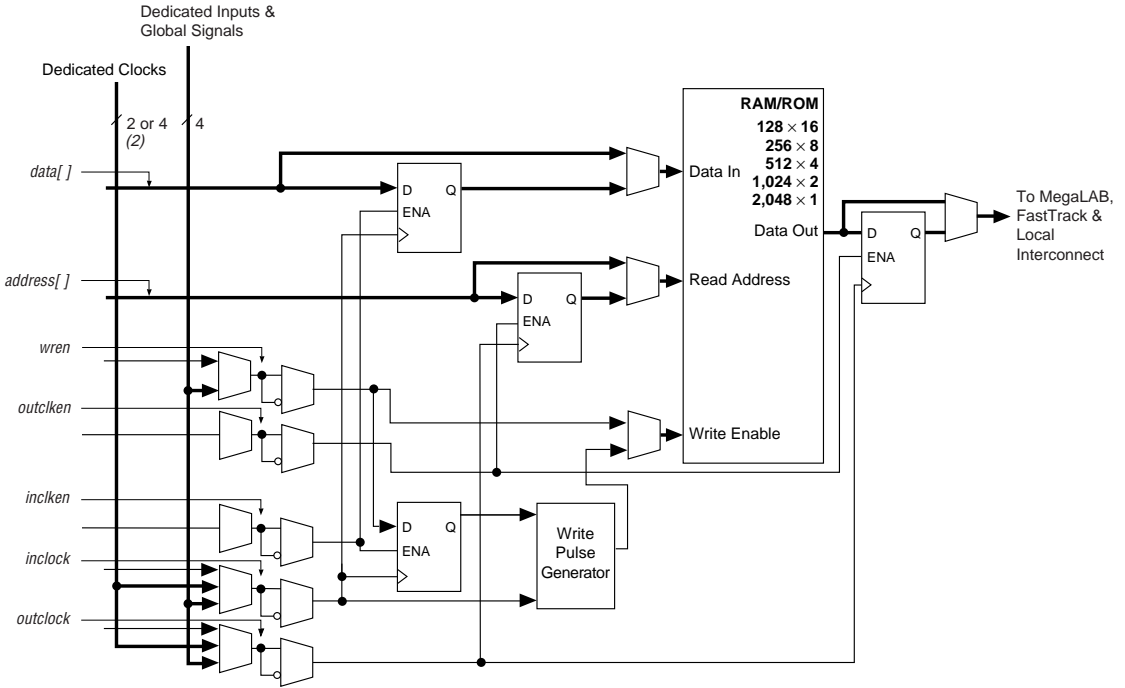
Notes:
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match-found flag is set high. Figure 23 shows the CAM block diagram.

Figure 23. APEX 20KE CAM Block Diagram

```
        wraddress[]              data_address[]
        data[]                          match
        wren                          outclock
        inclock                     outclocken
        inclocken                      outaclr
        inaclr
```
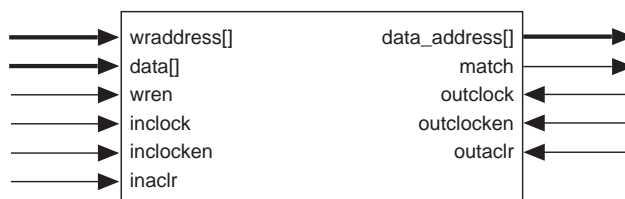
CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't-care" bits into words of the memory. The don't-care bit can be used as a mask for CAM comparisons; any bit set to don't-care has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output, because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will not be correct. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When don't-care bits are used, a third clock cycle is required.

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation
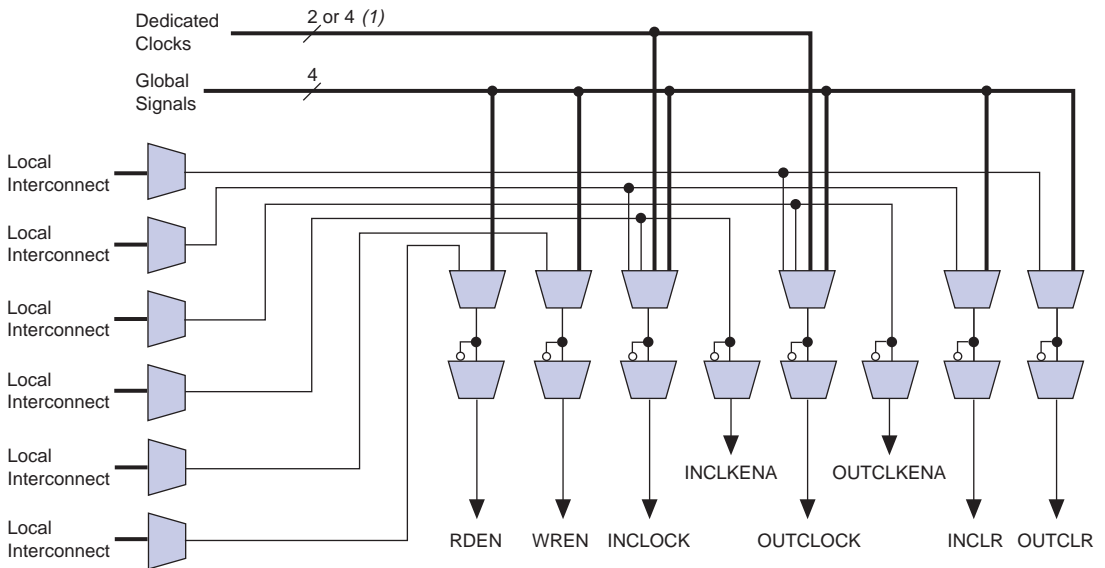
Note:
(1)   APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20K I/O element (IOE) contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The Quartus Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure a zero hold time. A path in which a pin directly drives a register may require the delay, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. The Quartus timing analyzer can provide guidance as to where positive hold times occur in a design; at those points, the delay should be turned on. Another programmable delay can be used to increase clock-to-output time for use when driving devices with a hold time requirement. Figure 25 shows the APEX 20K IOE.

The register in the APEX 20K IOE can be programmed to power up high or low after configuration is complete. If it is programmed to power up low, an asynchronous clear can control the register. If it is programmed to power up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25. APEX 20K Bidirectional I/O Registers
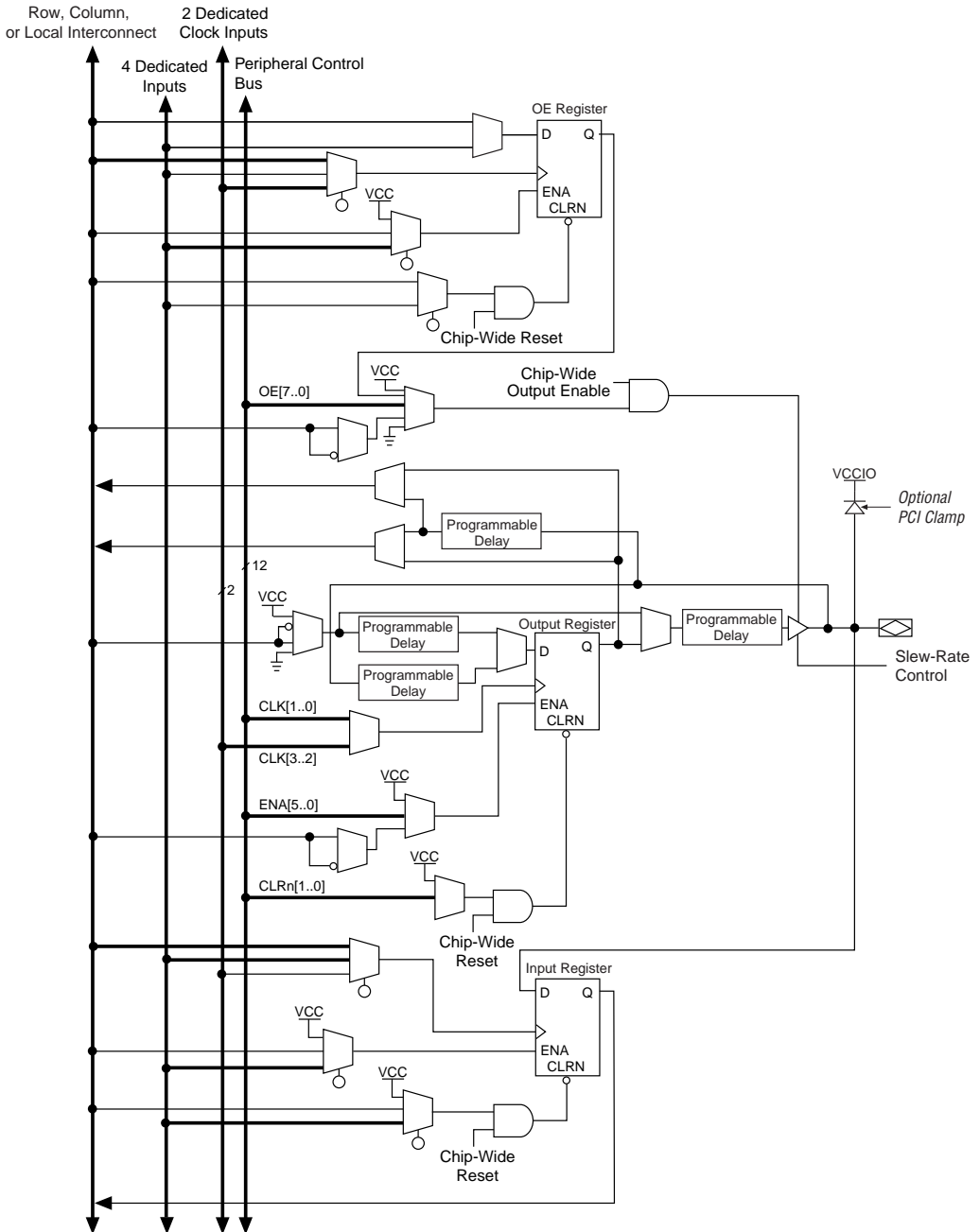
APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements.

The register in the APEX 20KE IOE can be programmed to power up high or low after configuration is complete. If it is programmed to power up low, an asynchronous clear can control the register. If it is programmed to power up high, an asynchronous preset can control the register. Figure 26 shows the APEX 20KE IOE. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 26. APEX 20KE Bidirectional I/O Registers
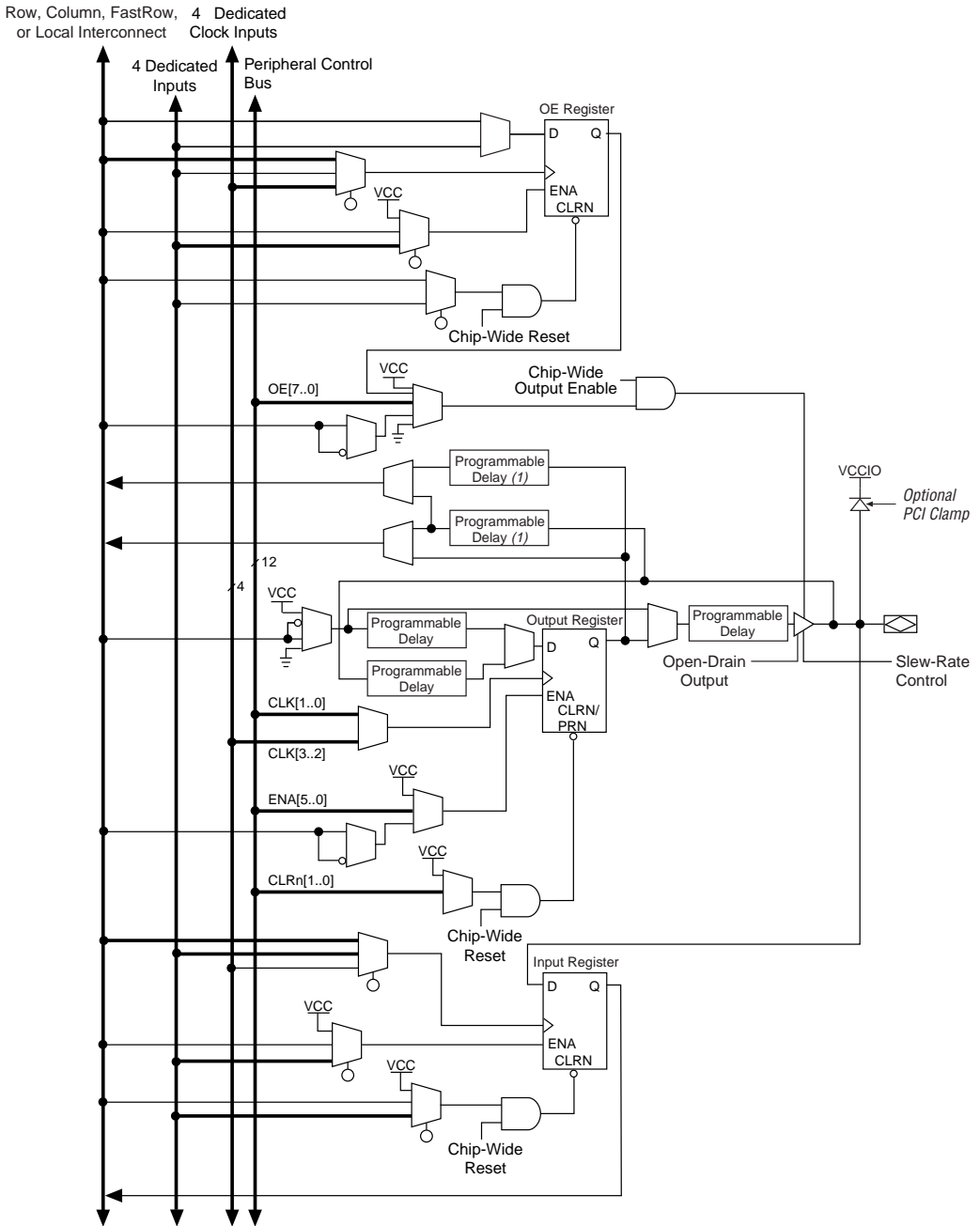
Note:

(1)   This programmable delay has four settings: off and three levels of delay.

Each IOE drives row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27 shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect
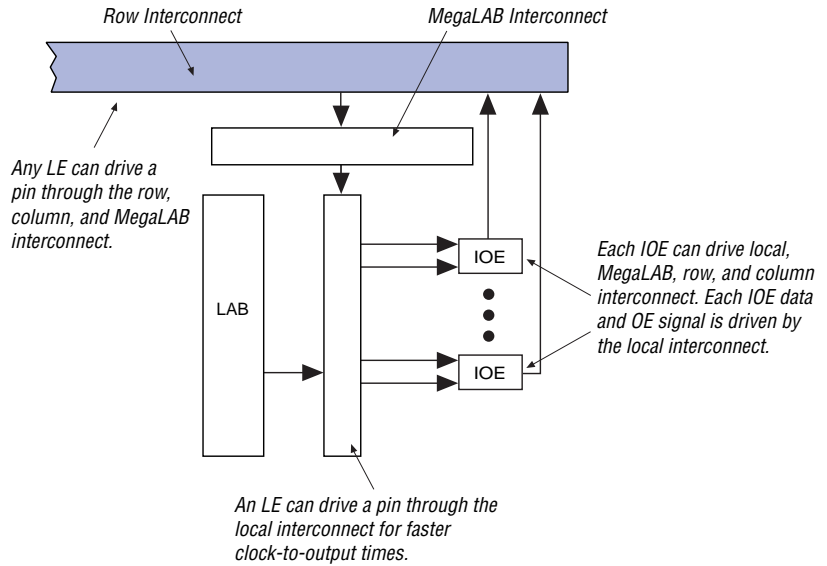
Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect

Each IOE can drive column interconnect. In APEX 20KE devices, IOEs can also drive FastRow and column interconnect. Each IOE data and OE signal is driven by local interconnect.

IOE   IOE

An LE or ESB can drive a pin through a local interconnect for faster clock-to-output times.

LAB

Any LE or ESB can drive a column pin through a row, column, and MegaLAB interconnect.

Column Interconnect

Row Interconnect   *MegaLAB Interconnect*

Advanced I/O Standard Support

The APEX 20KE IOE supports the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, 3.3-V AGP, LVDS, GTL+, SSTL-3 Class I and II, SSTL-2 Class I and II, and HSTL Class I, II, and III.

The APEX 20KE device contains eight I/O blocks. All blocks support all standards except LVDS. In addition, one block supports LVDS inputs, and another block supports LVDS outputs. Each I/O block has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each block can support a different standard independently. Each block can also use a separate V_{REF} level, so that each block can support any of the terminated standards (such as SSTL-3) independently. Within a block, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface.

When LVDS signals are used within a block, other I/O standards should not be used within the same block to avoid degrading the high-performance LVDS signal. An exception can be made for the ClockLock LOCK signal, which does not toggle during normal operation. Figure 29 shows the arrangement of the APEX 20KE I/O blocks.

Figure 29. APEX 20KE I/O Blocks
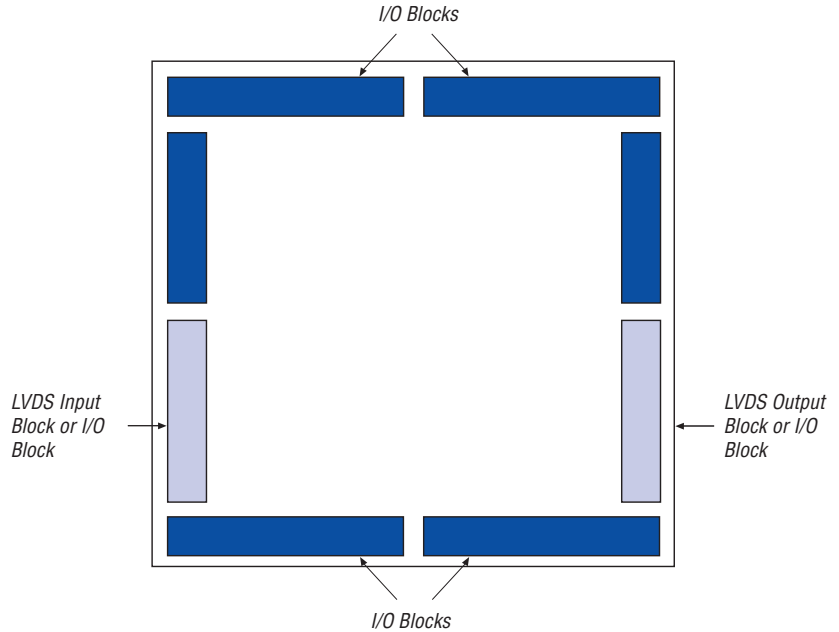
Power Sequencing & Hot Socketing

Because APEX 20K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power planes may be powered in any order.

Signals can be driven into APEX 20K devices before and during power up without damaging the device. In addition, APEX 20K devices do not drive out during power up. Once operating conditions are reached and the device is configured, APEX 20K devices operate as specified by the user.

SameFrame Pin-Outs

APEX 20K devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EP20K100 device in a 324-pin FineLine BGA package to an EP20K400 device in a 672-pin FineLine BGA package.

The Quartus software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Quartus software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 30).

Figure 30. SameFrame Pin-Out Example

Printed Circuit Board
Designed for 672-Pin FineLine BGA Package

324-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

672-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)
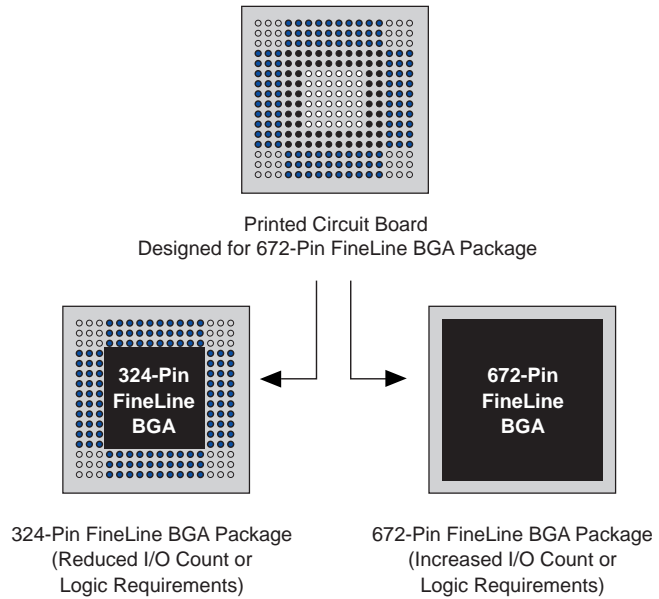
ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock trace; unlike ASICs, the user does not have to design and optimize the clock trace. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and bandwidth.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus software. External devices are not required to use these features.

In designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to GCLK1. Table 9 shows the combinations supported by the ClockLock and ClockBoost circuitry. The GCLK1 pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (GCLK0) cannot be used.

Table 9. Multiplication Factor Combinations

Clock 0	Clock 1
1×	2×
1×	4×
2×	4×

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM. When using external feedback, the PLL output can be multiplied. Also, the clock delay adjustment feature is available.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m, n, and k range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

In addition, two PLLs include special circuitry to support T1/E1 conversion. The T1 telecommunications standard uses a 1.544-MHz clock, and the E1 telecommunications standard uses a 2.048-MHz clock. These two PLLs can convert a T1 clock to an E1 clock, or vice versa.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by approximately 2 ns with 0.5-ns resolution.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 50 MHz to support 400 Mbits/second LVDS data transfer. In this example, the PLL multiplies the incoming clock by 8 to support the high-speed data transfer. The LVDS interface is supported by EP20K300E and larger devices.

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. Both signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 31 shows the incoming and generated clock specifications.

Figure 31. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.
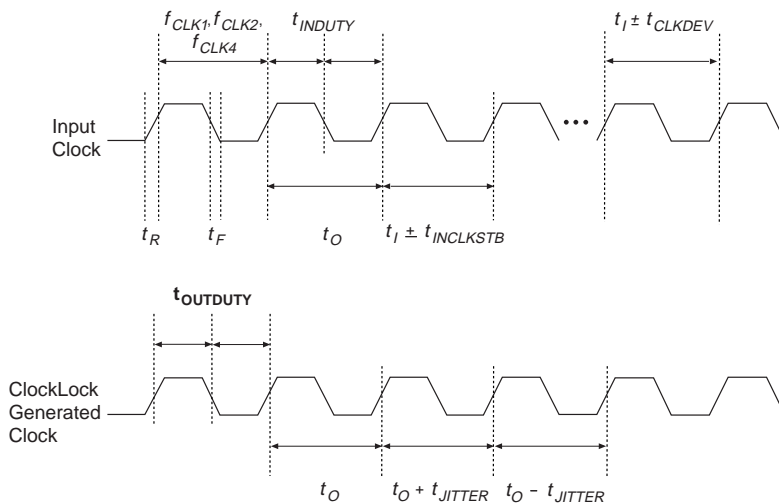
Table 10 summarizes the ClockLock and ClockBoost parameters for APEX 20K devices. Specifications for APEX 20KE devices will be released in a future data sheet.

Symbol	Parameter	Min	Typ	Max	Unit
t_R	Input rise time			5	ns
t_F	Input fall time			5	ns
t_{INDUTY}	Input duty cycle	40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25		133	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	20		66	MHz
f_{CLKDEV}	Input deviation from user specification in the Quartus software (ClockBoost clock multiplication factor equals 1) *(1)*			25,000 *(2)*	PPM
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	15		33	MHz
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)			100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*			10	μs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*			250 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock	40	50	60	%

Table 10. ClockLock & ClockBoost Parameters

Notes to table:

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus software, designers must specify the input frequency. The Quartus software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation. The maximum value for t_{JITTER} is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus software or via hardware using Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 11.

Table 11. APEX 20K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring an APEX 20K device via the JTAG port with a ByteBlasterMV download cable, or using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	These instructions monitor internal device operation with the SignalTap embedded logic analyzer.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 12 and 13 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 12. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K100	*(1)*
EP20K100E	*(1)*
EP20K160E	*(1)*
EP20K200	*(1)*
EP20K200E	*(1)*
EP20K300E	*(1)*
EP20K400	1,536
EP20K400E	*(1)*
EP20K600E	*(1)*
EP20K1000E	*(1)*

Note:
(1) Consult Altera Applications for up-to-date information on this device.

Table 13. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) (2)
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	(3)	(3)	000 0110 1110	1
EP20K160E	(3)	(3)	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	(3)	(3)	000 0110 1110	1
EP20K300E	(3)	(3)	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	(3)	(3)	000 0110 1110	1
EP20K600E	(3)	(3)	000 0110 1110	1
EP20K1000E	(3)	(3)	000 0110 1110	1

Notes:

(1)   The most significant bit (MSB) is on the left.

(2)   The IDCODE's least significant bit (LSB) is always 1.

(3)   Consult Altera Applications for up-to-date information on this device.

Figure 32 shows the timing requirements for the JTAG signals.

Figure 32. APEX 20K JTAG Waveforms
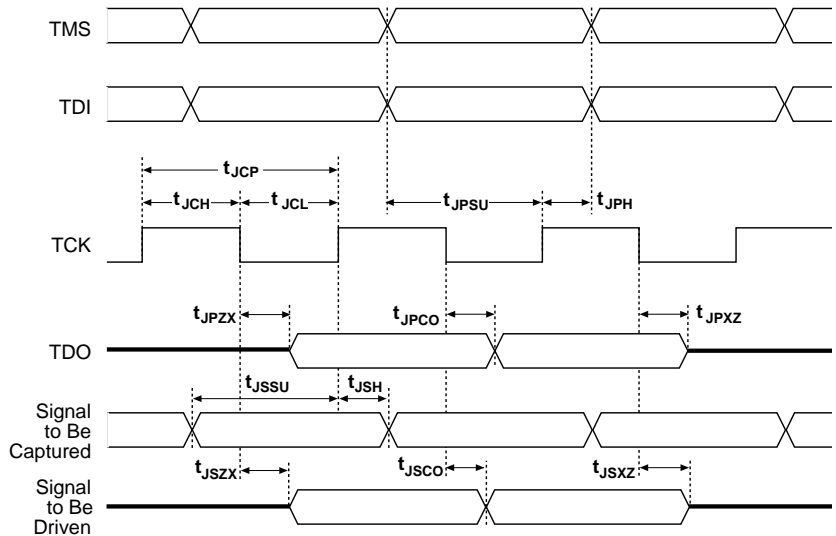
Table 14 shows the JTAG timing parameters and values for APEX 20K devices.

Symbol	Parameter	Min	Max	Unit
Table 14. APEX 20K JTAG Timing Parameters & Values				
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing   Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 33. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 33. APEX 20K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Device Output — To Test System

Device input rise and fall times < 3 ns

C1 (includes JIG capacitance)
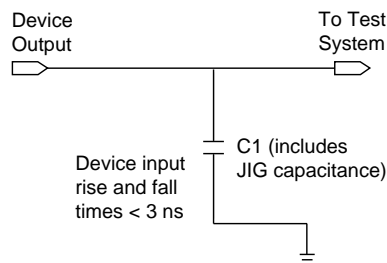
Operating Conditions

Tables 15 through 18 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices. Consult Altera for specifications on 1.8-V APEX 20KE devices.

Table 15. APEX 20K Device Absolute Maximum Ratings   *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	−0.5	3.6	V
V_{CCIO}			−0.5	4.6	V
V_I	DC input voltage		−2.0	4.6	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 16. APEX 20K Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3), (4)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3), (4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*(5)*	−0.5	4.1	V

Table 16. APEX 20K Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 17. APEX 20K Device DC Operating Conditions (Part 1 of 2)   *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, $0.5 \times V_{CCIO}$ *(8)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		−0.5		0.7, $0.3 \times V_{CCIO}$ *(8)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = −12 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	I_{OH} = −0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	I_{OH} = −0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = −1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = −2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.45	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = −12 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to −0.5 V	−10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to −0.5 V	−10		10	µA

Table 17. APEX 20K Device DC Operating Conditions (Part 2 of 2)   *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(11)*	20		50	kΩ
		V_{CCIO} = 2.3 V *(11)*	30		80	kΩ

Table 18. APEX 20K Device Capacitance   *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:
(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20K device recommended operating conditions, shown in Table 16 on page 74.
(8) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS). Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 34 on page 77.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Figure 34 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance.

Figure 34. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance
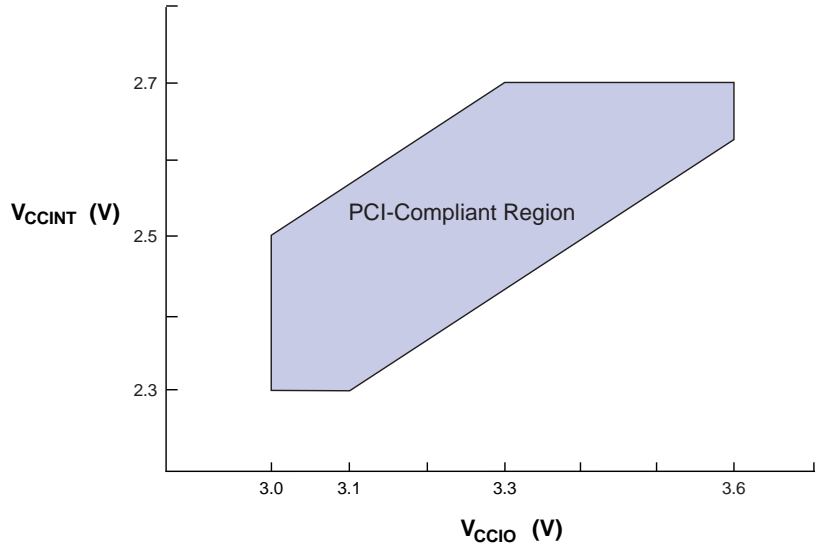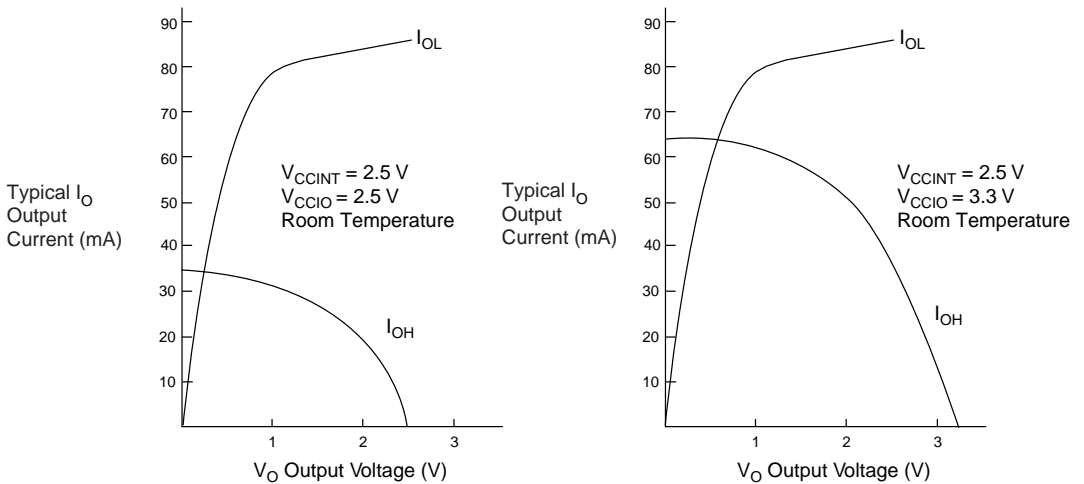

Figure 35 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when VCCIO pins are connected to 3.3 V).

*Figure 35. Output Drive Characteristics of APEX 20K Devices*

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Timing simulation and delay prediction are available with the Quartus Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 1-ps resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis. Figure 36 shows the timing model for bidirectional I/O pin timing.

Figure 36. Synchronous Bidirectional Pin External Timing Model
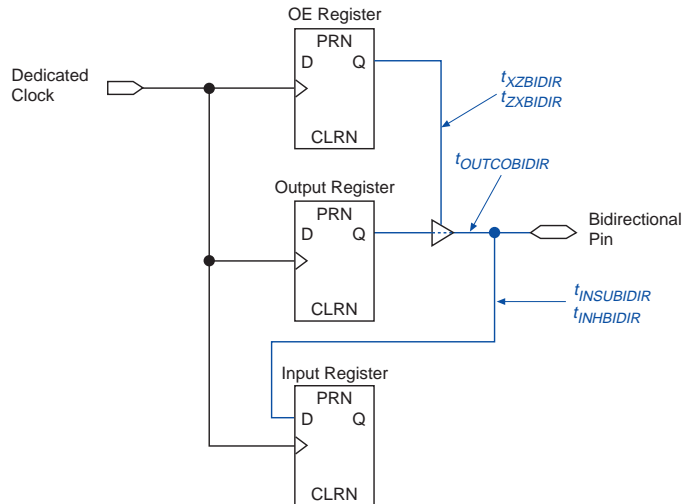
Tables 19 and 20 define the I/O timing parameters for APEX 20K devices. Tables 21 through 26, show the I/O timing parameter values for APEX 20K devices.

Table 19. External Timing Parameters		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	

Table 20. External Bidirectional Timing Parameters

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 35 pF

Table 21. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.1		2.5		3.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.0	2.0	4.1	2.0	5.5	ns
t_{INSU} (2)	2.1		2.5		3.0		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	3.0	0.5	3.1	0.5	4.5	ns

Notes:

(1)   This parameter is measured without use of the ClockLock or ClockBoost circuits.

(2)   This parameter is measured with use of the ClockLock or ClockBoost circuits.

Table 22. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.1		1.5		2.2		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.0	2.0	4.1	2.0	5.5	ns
$t_{XZBIDIR}$ (1)		4.8		5.8		6.8	ns
$t_{ZXBIDIR}$ (1)		5.9		7.1		8.3	ns
$t_{INSUBIDIR}$ (2)	1.1		1.5		2.2		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.0	0.5	3.1	0.5	4.5	ns
$t_{XZBIDIR}$ (2)		3.8		4.8		5.8	ns
$t_{ZXBIDIR}$ (2)		4.9		6.1		7.3	ns

Notes:
(1)   This parameter is measured without use of the ClockLock or ClockBoost circuits.
(2)   This parameter is measured with use of the ClockLock or ClockBoost circuits.

Table 23. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.1		2.5		3.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.0	2.0	4.1	2.0	5.5	ns
t_{INSU} (2)	2.1		2.5		3.0		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	3.0	0.5	3.1	0.5	4.5	ns

Notes:
(1)   This parameter is measured without use of the ClockLock or ClockBoost circuits.
(2)   This parameter is measured with use of the ClockLock or ClockBoost circuits.

Table 24. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.2		1.5		2.1		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.0	2.0	4.1	2.0	5.5	ns
$t_{XZBIDIR}$ (1)		4.8		5.8		6.8	ns
$t_{ZXBIDIR}$ (1)		5.9		7.1		8.3	ns
$t_{INSUBIDIR}$ (2)	1.2		1.5		2.1		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.0	0.5	3.1	0.5	4.5	ns
$t_{XZBIDIR}$ (2)		3.8		4.8		5.8	ns
$t_{ZXBIDIR}$ (2)		4.9		6.1		7.3	ns

Notes:
(1)   This parameter is measured without use of the ClockLock or ClockBoost circuits.
(2)   This parameter is measured with use of the ClockLock or ClockBoost circuits.

Table 25. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.1		2.5		3.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.0	2.0	4.1	2.0	5.5	ns
t_{INSU} (2)	2.1		2.5		3.0		ns
t_{INH} (2)	0.0		0.0		0.0		ns
t_{OUTCO} (2)	0.5	3.0	0.5	3.1	0.5	4.5	ns

Notes:
(1)   This parameter is measured without use of the ClockLock or ClockBoost circuits.
(2)   This parameter is measured with use of the ClockLock or ClockBoost circuits.

Table 26. EP20K400 External Bidirectional Timing Parameters							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$ (1)	1.2		1.5		1.8		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.0	2.0	4.1	2.0	5.5	ns
$t_{XZBIDIR}$ (1)		4.9		5.8		6.9	ns
$t_{ZXBIDIR}$ (1)		6.0		7.1		8.4	ns
$t_{INSUBIDIR}$ (2)	1.2		1.5		1.8		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.0	0.5	3.1	0.5	4.5	ns
$t_{XZBIDIR}$ (2)		3.9		4.8		5.9	ns
$t_{ZXBIDIR}$ (2)		5.0		6.1		7.4	ns

Notes:
(1)   This parameter is measured without use of the ClockLock or ClockBoost circuits.
(2)   This parameter is measured with use of the ClockLock or ClockBoost circuits.

Power Consumption

Detailed power consumption information for APEX 20K devices will be released as it is available.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration all I/Os are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 27), chosen on the basis of the target application. An EPC2 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When an EPC2 configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 27. Data Sources for Configuration	
Configuration Scheme	**Data Source**
Configuration device	EPC2 configuration device
Passive serial (PS)	ByteBlasterMV download cable, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	ByteBlasterMV download cable, or a microprocessor with a Jam or JBC File

Device Pin-Outs

Table 28 shows the pin names and numbers for EP20K400 devices in 652-pin BGA and 655-pin PGA packages.

Table 28. EP20K400 Device Pin-Outs (Part 1 of 2) Note (1)		
Pin Name	**652-Pin BGA**	**655-Pin PGA**
MSEL0 (2)	U35	A23
MSEL1 (2)	W35	C23
NSTATUS (2)	AN17	AE41
NCONFIG (2)	W32	C25
DCLK (2)	U3	BA23
CONF_DONE (2)	AM17	AC47
INIT_DONE (3)	C16	AE7
nCE (2)	U1	BE25
nCEO (2)	C19	AC9
nWS (4)	M1	BF14
nRS (4)	N1	AY20
nCS (4)	P2	BB20
CS (4)	R2	BD20
RDYnBSY (4)	A14	AH4
CLKUSR (4)	C15	AH6
DATA7 (4)	M6	BG13
DATA6 (4)	L6	BB16
DATA5 (4)	E7	BC3
DATA4 (4)	B5	AR7
DATA3 (4)	B7	AV4
DATA2 (4)	A8	AP6
DATA1 (4)	C13	AH8
DATA0 (2), (5)	U4	BE23
TDI (2)	W1	BG23
TDO (2)	C17	AE1
TCK (2)	AN19	AC45
TMS (2)	AM19	AD40
TRST (2)	D19	AD2
Dedicated Inputs	AP17, AP19, B17, B19	AB4, AC5, AC43, AE43
Dedicated Clock Pins	W34, U2	H24, AY24
LOCK (6)	AB6	BG29
GCLK1 (7)	U2	AY24
DEV_CLRn (3)	T6	AY22

Table 28. EP20K400 Device Pin-Outs (Part 2 of 2)		*Note (1)*
Pin Name	**652-Pin BGA**	**655-Pin PGA**
DEV_OE *(3)*	Y5	BF26
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31, W33	A3, A45, B24, C1, C11, C19, C29, C37, C47, D24, G47, L3, L45, N1, N47, W3, W45, AA1, AA47, AD4, AD44, AG1, AG47, AJ3, AJ45, AR1, AR47, AU3, AU45, AY8, BA1, BA47, BD24, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45
VCCIO	AL17, AL19, AL3, AL31, AL32, AL4, AM5, AN32, AN33, AN4, C32, C4, D31, D5, E17, E19, E3, E4, F30, F31, U30, U6, W30, W6	E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39
VCC_CKLK *(8)*	W4	BD28
GNDINT	D17, A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V35, V4, V5, V6	AD8, A47, B2, C13, C21, C27, C35, C45, D4, F24, J1, J47, N3, N45, R1, R47, W1, W47, AA3, AA45, AD6, AD42, AG3, AG45, AJ1, AJ47, AN1, AN47, AR3, AR45, AW1, AW47, BB24, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47
GNDIO	–	E7, E13, E19, E29, E35, E41, G5, G43, H40, N5, N43, W5, W43, AJ5, AJ43, AR5, AR43, AY40, BA5, BA43, BC7, BC13, BC19, BC29, BC35, BC41, BF46
GND_CKLK *(8)*	W2	BD26
No Connect (N.C.)	–	–
Total User I/O Pins *(9)*	502	502

Notes to table:
(1)   All pins that are not listed are user I/O pins.
(2)   This pin is a dedicated pin; it is not available as a user I/O pin.
(3)   This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4)   This pin can be used as a user I/O pin after configuration.
(5)   This pin is tri-stated in user mode.
(6)   This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(7)   This pin drives the ClockLock and ClockBoost circuitry.
(8)   This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(9)   The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.